1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 128 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software:

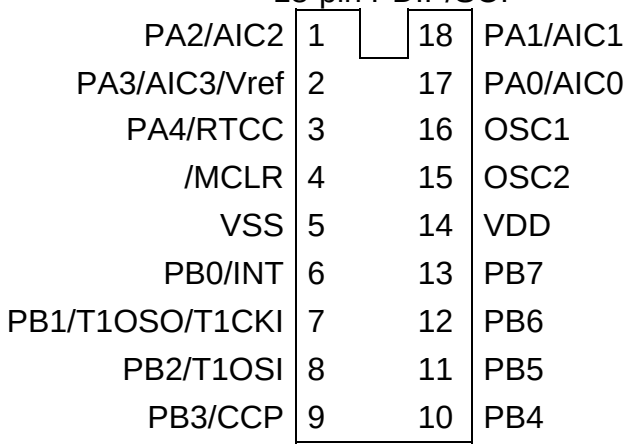
- Fully CMOS static design
- 8-bit data bus
- On chip EPROM size: 1.0 K words
- Internal RAM size: 128 bytes
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage:2.5V~5.5V(PRD disable)
  4.5V~5.5V(PRD enable)
- Operating frequency: DC ~ 20 MHz
- The most fast execution time is 200 ns under 20MHz in all single cycle instructions except the branch instruction
- Addressing modes include direct, indirect and relative addressing modes
- Power-on Reset
- Power edge-detector Reset
- Power range-detector Reset
- Sleep Mode for power saving
- Capture, Compare, PWM module
- 7 interrupt sources:
  -External INT pin
  -TMR0 timer, TMR1 timer, TMR2 timer
  -A/D conversion completion
  -PortB<7:4> interrupt on change
  -CCP
- A/D converter module:
  -4 analog inputs multiplexed into one A/D converter
  -8-bit resolution
- TMR0: 8-bit real time clock/counter
  TMR1: 16-bit real time clock/counter
  TMR2: 8-bit clock/counter
- 4 types of oscillator can be selected by programming option:
  RC－Low cost RC oscillator
  LFXT－Low frequency crystal oscillator
  XTAL－Standard crystal oscillator
  HFXT－High frequency crystal oscillator
- On-chip RC oscillator based Watchdog Timer (WDT)
- 13 I/O pins with their own independent direction control

3. Applications

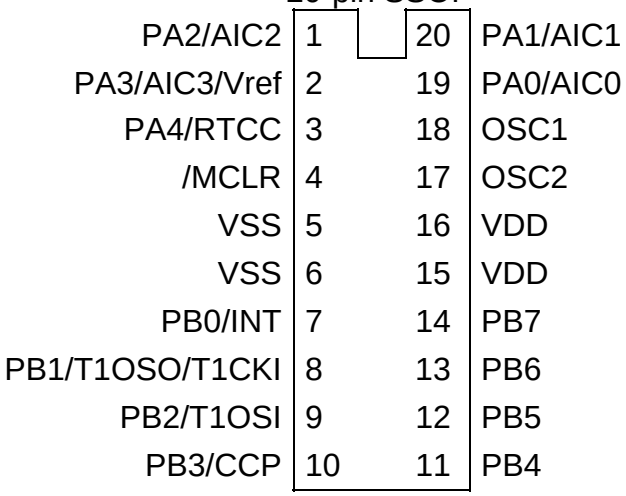
The application areas of this MDT10P712 range from appliance motor control and high speed auto-motive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

18-pin PDIP/SOP



20-pin SSOP



5. Pin Function Description

Pin Name	I/O	Function Description
PA0~PA3	I/O	Port A, TTL input level, Analog input channel.
PA4/RTCC	I/O	Real Time Clock/Counter, Schmitt Trigger input level. Open drain output.
PB0~PB7	I/O	Port B, TTL input level, PB0: External Interrupt input. PB4~PB7: Interrupt on pin change.
/MCLR	I	Master Clear, Schmitt Trigger input level.
OSC1/CLKIN	I	Oscillator Input, External clock input.
OSC2/CLKOUT	O	Oscillator Output, In RC mode, the CLKOUT pin has 1/4 frequency of CLKIN.
VDD		Power supply
VSS		Ground

6. Memory Map

(A) Register Map

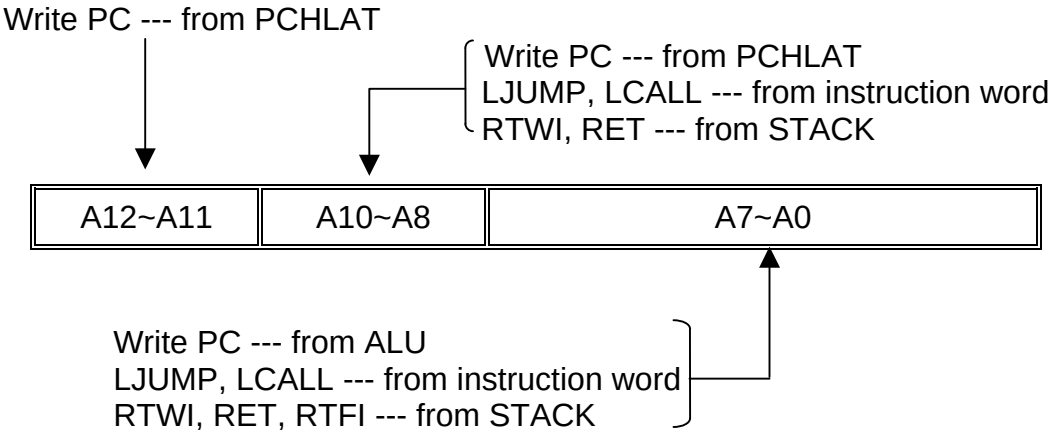
Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
07	DATACCP
0A	PCHLAT
0B	INTS
0C	PIFB1
0E	TMR1L
0F	TMR1H
10	T1STA
11	TMR2
12	T2STA
15	CCPL
16	CCPH
17	CCPCTL
1E	ADRES
1F	ADS0
20~7F	General purpose register
BANK1	
81	TMR
85	CPIO A
86	CPIO B
87	CPIOCCP
8C	PIEB1
8E	PSTA

Address	Description
92	T2PER
9F	ADS1
A0~BF	General purpose register

(1) IAR (Indirect Address Register): R00

(2) RTCC (Real Time Counter/Counter Register): R01

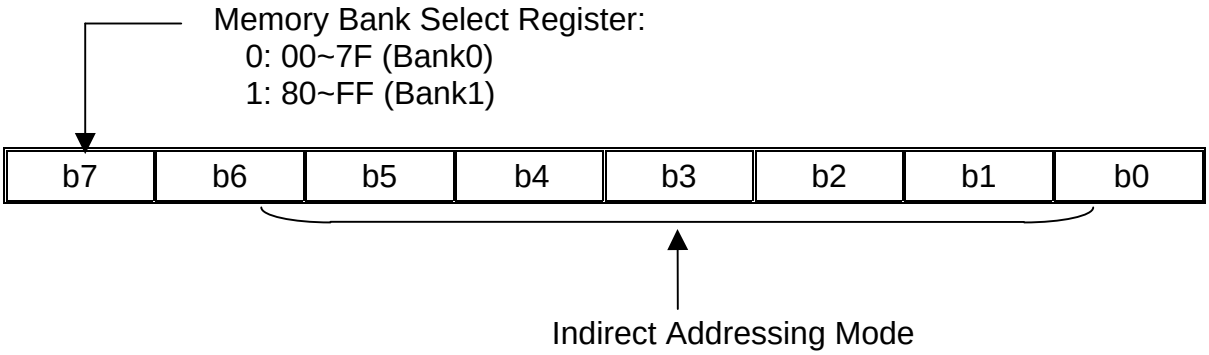
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power down Flag bit
4	TF	WDT Timer overflow Flag bit
5	RBS0	Register Bank Select bit: 0: 00H --- 7FH (Bank0) 1: 80H --- FFH (Bank1)
7-6	——	General purpose bit

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05

PA4~PA0, I/O Register

(7) PORT B: R06

PB7~PB0, I/O Register

(8) DATACCP: R07

Bit	Symbol	Function
0	DT1CK	T1CKI PIN. Controlled from software.
1	--	Unimplemented
2	DCCP	CCP1 PIN. Controlled from software.
7~3	--	Unimplemented

(9) PCHLAT: R0A

(10) INTS (Interrupt Status Register): R0B

Bit	Symbol	Function
0	RBIF	PORTB<7~4> pin change interrupt flag.
1	INTF	Set when INT interrupt occurs. INT interrupt flag.
2	TIF	Set when TMR0 overflows.
3	RBIE	0: disable PB change interrupt. 1: enable PB change interrupt.
4	INTS	0: disable INT interrupt. 1: enable INT interrupt.
5	TIS	0: disable TMR0 interrupt. 1: enable TMR0 interrupt.
6	PEIE	0: disable all peripheral interrupt. 1: enable all peripheral interrupt.
7	GIS	0: disable global interrupt. 1: enable global interrupt.

(11) PIFB1 (Peripheral Interrupt Flag Bit): R0C

Bit	Symbol	Function
0	TMR1IF	TMR1 interrupt flag 0: TMR1 did not overflow 1: TMR1 overflowed
1	TMR2IF	TMR2 interrupt flag 0: No TMR2 to T2PER match occurred 1: TMR2 to T2PER match occurred
2	CCPIF	CCP interrupt flag 0: No TMR1 capture/compare occurred 1: A TMR1 capture/compare occurred
5~3	--	Unimplemented
6	ADIF	A/D interrupt flag 0: A/D conversion is not complete 1: A/D conversion completed
7	--	Unimplemented

(12) TMR1L: R0E

The LSB of the 16-bit TMR1

(13) TMR1H: R0F

The MSB of the 16-bit TMR1

(14) T1STA: R10

Bit	Symbol	Function
0	TMR1ON	0: Stop TMR1. 1: enable TMR1.
1	TMR1CLK	0: Internal clock (Fosc/4). 1: External clock from pin PB2.
2	/T1SYNC	TMR1CLK = 1 0: Synchronize external clock. 1: Do not synchronize external clock. TMR1CLK = 0 This bit is ignored.
3	T1OSCEN	0: TMR1 Oscillator is shut off. 1: TMR1 Oscillator is enable.

Bit	Symbol	Function
5~4	T1CKPS1 ~ T1CKPS0	1 1 = 1:8 Prescale value 1 0 = 1:4 Prescale value 0 1 = 1:2 Prescale value 0 0 = 1:1 Prescale value
7~6	--	Unimplemented

(15) TMR2: R11

TMR2 register

(16) T2STA: R12

Bit	Symbol	Function
1~0	T2CKPS1 ~ T2CKPS0	0 0 = Prescaler is 1 0 1 = Prescaler is 4 1 x = Prescaler is 16
2	TMR2ON	0: TMR2 is on. 1: TMR2 is off.
7~3	--	Unimplemented

(17) CCPL: R15

Capture/Compare/PWM LSB

(18) CCPH: R16

Capture/Compare/PWM MSB

(19) CCPCTL: R17

Bit	Symbol	Function
3~0	CCPM3 ~ CCPM0	0 0 0 0: CCP off. 0 1 0 0: Capture mode, every falling edge. 0 1 0 1: Capture mode, every rising edge. 0 1 1 0: Capture mode, every 4th rising edge. 0 1 1 1: Capture mode, every 16th rising edge. 1 0 0 0: Compare mode, set output on match. 1 0 0 1: Compare mode, clear output on match. 1 0 1 0: Compare mode, generate software interrupt on match. 1 0 1 1: Compare mode, trigger special event. 1 1 x x: PWM mode.
5~4	PWMLSB	These bits are the two LSBs of the PWM duty cycle.
7~6	--	Unimplemented

(20) ADRES (A/D result register) : R1E

(21) ADS0 (A/D Status Register) : R1F

Bit	Symbol	Function
0	ADRUN	0: A/D converter module is shut off and consumes no operating current. 1: A/D converter module is operating.
1	--	Unimplemented
2	GO/DONEB	0: A/D conversion in progress. 1: A/D conversion not in progress.
5~3	CHS2~0	000: AIC0, 001: AIC1, 010: AIC2, 011: AIC3
7~6	ASCS1-0	00: fosc/2, 01: fosc/8, 10: fosc/32, 11: f RC (*Note)

*Note: determined by OSC mode, HF: fosc/32, XT: fosc/8, RC: fosc/2, LF: fosc/2

(22) TMR (Time Mode Register): R81

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2~0	PS2~0	0 0 0	1: 2	1: 1
		0 0 1	1: 4	1: 2
		0 1 0	1: 8	1: 4
		0 1 1	1: 16	1: 8
		1 0 0	1: 32	1: 16
		1 0 1	1: 64	1: 32
		1 1 0	1: 128	1: 64
		1 1 1	1: 256	1: 128
3	PSC	Prescaler assignment bit: 0: RTCC 1: Watchdog Timer		
4	TCE	RTCC signal Edge: 0: Increment on low-to-high transition on RTCC pin. 1: Increment on high-to-low transition on RTCC pin.		
5	TCS	RTCC signal set: 0: Internal instruction cycle clock. 1: Transition on RTCC pin.		
6	IES	Interrupt edge select: 0: Interrupt on falling dege on PB0. 1: Interrupt on rising edge on PB0.		
7	PBPH	PORTB pull-hi: 0: PORTB pull-hi enable. 1: PORTB pull-hi disable.		

(23) CPIO A (Control Port I/O Mode Register): R85
=“0”, I/O pin in output mode.
=“1”, I/O pin in input mode.

(24) CPIO B (Control Port I/O Mode Register): R86
=“0”, I/O pin in output mode.
=“1”, I/O pin in input mode.

(25) CPIOCCP: R87

Bit	Symbol	Function
0	CT1CK	0: T1CKI pin is an output. 1: T1CKI pin is an input.
1	--	Unimplemented
2	CCCP	0: Output pin driven. 1: Output pin tristated.
7~3	--	Unimplemented

(26) PIEB1: R8C

Bit	Symbol	Function
0	TMR1IE	TMR1 interrupt enable bit 0: disable TMR1 interrupt. 1: enable TMR1 interrupt.
1	TMR2IE	TMR2 interrupt enable bit 0: disable TMR2 interrupt. 1: enable TMR2 interrupt.
2	CCPIE	CCP interrupt enable bit 0: disable CCP interrupt. 1: enable CCP interrupt.
5~3	--	Unimplemented
6	ADIE	A/D interrupt enable bit 0: disable A/D interrupt. 1: enable A/D interrupt.
7	--	Unimplemented

(27) PSTA: R8E

Bit	Symbol	Function
0	PRDB	0: Power range-detector Reset occurred. 1: No Power range-detector Reset Occurred.
1	PORB	0: Power on Reset occurred. 1: No Power on Reset occurred.

(28) T2PER: R92
Timer2 period

(29) ADS1 (A/D Status Register): R9F

Bit	Symbol	Function
2~0	PAVM2~0	0 x 0: PA0~3= analog input. VREF= VDD. 0 x 1: PA0~2= analog input. PA3= ref input. VREF= PA3. 1 0 0: PA0, 1, 3= analog input. PA2= digital I/O. VREF= VDD. 1 0 1: PA0, 1= analog input. PA2= digital I/O, PA3= ref input, VREF= PA3. 1 1 x: PA0~3= digital I/O.

(30) Configurable options for EPROM (Set by writer):

Oscillator Type
RC Oscillator
HFXT Oscillator
XTAL Oscillator
LFXT Oscillator

Watchdog Timer control
Watchdog timer disable all the time
Watchdog timer enable all the time

Power-range control
Power-range disable
Power-range enable

Oscillator-start Timer control
0ms
80ms

Power-edge Detect
PED Disable
PED Enable

Security state
Security Disable
Security Enable

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.
004	Interrupt vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000 0000	0000 0000	PC+1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	---x xxxx	---u uuuu	---u uuuu
PORT B	06h	xxxx xxxx	uuuu uuuu	uuuu uuuu
DATACCP	07h	---- -x-x	---- -u-u	---- -u-u
PCHLAT	0Ah	---0 0000	---0 0000	---u uuuu
INTS	0Bh	0000 000x	0000 000u	uuuu uuuu
PIFB1	0Ch	-0-- 0000	-0-- 0000	-u-- uuuu
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1STA	10h	--00 0000	--uu uuuu	--uu uuuu
TMR2	11h	0000 0000	0000 0000	uuuu uuuu
T2STA	12h	---- -000	---- -uuu	---- -uuu
CCPL	15h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPH	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPCTL	17h	--00 0000	--00 0000	--uu uuuu
ADRES	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS0	1Fh	0000 00-0	0000 00-0	uuuu uu-u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	---1 1111	---1 1111	---u uuuu
CPIOB	86h	1111 1111	1111 1111	uuuu uuuu

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
CPIOCCP	87h	xxxx x1x1	xxxx x1x1	xxxx xuxu
PIEB1	8Ch	-0-- 0000	-0-- 0000	-u-- uuuu
PSTA	8Eh	---- --0u	---- --uu	---- --uu
T2PER	92h	1111 1111	1111 1111	1111 1111
ADS1	9Fh	---- -000	---- -000	---- -uuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3	PSTA: bit 1	PSTA: bit 0
/MCLR reset (not during sleep)	u	u	u	u
/MCLR reset during sleep	1	0	u	u
WDT reset (not during sleep)	0	1	u	u
WDT reset during sleep	0	0	u	u
Power-on reset	1	1	0	x
Power-range reset	1	1	u	0

8. Instruction Set:

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000100	RET	Return from subroutine	Stack→PC	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)] →t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z

Instruction Code	Mnemonic Operands	Function	Operating	Status
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI i	Add immediate to W	W+i→W	C,HC,Z
110001 iiiiiiii	RTWI i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI i	Subtract W from immediate	i-W→W	C,HC,Z
010000 00001001	RTFI	Reture from interrupt	Stack→PC,1→GIS	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register		0	: Working register
CPIO	:	Control I/O port register		1	: General register
TF	:	Timer overflow flag	R	:	General register address
PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry

OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	i	:	Immediate data (8 bits)
			n	:	Immediate address

9. Electrical Characteristics

*Note: Temperature=25°C

1.Operation Current :

(1) HF (C=10p) , WDT – enable , PRD – disable

	4M	10M	20M	Sleep
2.5V	420uA	910uA	1.5mA	6uA
3.0V	560uA	1.1mA	2mA	10uA
4.0V	950uA	1.8mA	3mA	20uA
5.0V	1.5mA	2.6mA	4.5mA	30uA
5.5V	2.4mA	3.9mA	7.3mA	50uA

These parameters are for reference only.

(2) XT (C=10p) , WDT – enable , PRD – disable

	1M	4M	10M	Sleep
2.5V	140uA	350uA	900uA	6uA
3.0V	180uA	460uA	1.1mA	10uA
4.0V	360uA	790uA	1.8mA	20uA
5.0V	730uA	1.3mA	2.6mA	30uA
5.5V	1.5mA	2mA	3.8mA	50uA

These parameters are for reference only.

(3) LF (C=10p) , WDT – enable , PRD – disable

	32K	455K	1M	Sleep
2.5V	16uA	65uA	90uA	6uA
3.0V	26uA	84uA	140uA	10uA
4.0V	110uA	160uA	240uA	20uA
5.0V	610uA	260uA	360uA	30uA
5.5V	---uA	480uA	630uA	50uA

These parameters are for reference only.

(4) RC , WDT – enable , PRD – disable , @Vdd = 5.0V

C	R	Freq.	Current
3p	4.7k	8.7M	2.3mA
	10k	4.5M	1.3mA
	47k	1M	470uA
	100k	495K	330uA
	300k	167K	260uA
	470k	105K	240uA
20p	4.7k	5.1M	1.4mA
	10k	2.6M	840uA
	47k	580K	370uA
	100k	277K	300uA
	300k	93K	260uA
	470k	59K	250uA
100p	4.7k	2M	710uA
	10k	1M	470uA
	47k	224K	280uA
	100k	107K	250uA
	300k	36K	240uA
	470k	22K	240uA
300p	4.7k	913K	450uA
	10k	445K	320uA
	47k	98K	240uA
	100k	46K	230uA
	300k	16K	220uA
	470k	10K	220uA

These parameters are for reference only.

2. Input Voltage (Vdd = 5V) :

	Port	Min	Max
Vil	TTL	Vss	1V
	Schmitt trigger	Vss	1V
Vih	TTL	2V	Vdd
	Schmitt trigger	3.5V	Vdd

These parameters are for reference only.

3. Output Voltage (Vdd = 5V) :

	PA,PB	Condition
Voh	3.2V	Ioh =-20mA
Vol	0.8V	Iol =+20mA
Voh	4.3V	Ioh = -5mA
Vol	0.5V	Iol = +5mA

These parameters are for reference only.

4. Output Current (Max.) (Vdd = 5V) :

Port A:

	Current
Source current	25mA
Sink current	25mA

These parameters are for reference only.

Port B:

	Current
Source current	25mA
Sink current	25mA

These parameters are for reference only.

5. The basic WDT time-out cycle time :

	Time
2.5V	24ms
3.0V	22ms
4.0V	20ms
5.0V	18ms
5.5V	17ms

These parameters are for reference only.